IN THE CLAIMS

1. (Currently amended) A network processor integrated circuit comprising: ~~An apparatus for use in a processor for controlling access of a plurality of processor clients to a plurality of memory instances of an internal memory of the processor, the apparatus comprising:~~

a plurality of processor clients internal to the network processor integrated circuit;

an internal memory having a plurality of memory instances; and

an internal memory controller for controlling access of the plurality of processor clients to the plurality of memory instances, the internal memory controller comprising a configurable switching element;

the configurable switching element being connectable between the plurality of processor clients and the plurality of memory instances and being operative to control access of particular ones of the plurality of processor clients to particular ones of the plurality of memory instances;

wherein the configurable switching element is configurable to connect any one of at least a subset of the plurality of processor clients to each of at least a subset of the plurality of memory instances,

such that in a first selectable configuration of the configurable switching element, a given one of the processor clients is permitted to access a first set of memory instances comprising one or more of the plurality of memory instances, and in a second selectable configuration of the configurable switching element, the given processor client is permitted to access a second set of memory instances comprising one or more of the plurality of memory instances, the second set being different than the first set.

2. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 1 wherein the configurable switching element comprises a configurable crossbar having a first set of ports coupled to the plurality of processor clients and a second set of ports coupled to the plurality of memory instances.

3. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 1 wherein the memory controller further comprises control circuitry operative to control selection of a particular configuration for the configurable switching element.

4. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 3 wherein the control circuitry further comprises an address control circuit.

5. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 3 wherein the control circuitry further comprises a data multiplexing control circuit.

6. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 1 wherein the internal memory controller further comprises a configuration interface providing an interface between the configurable switching element and a configuration source external to the memory controller, the external configuration source providing to the memory controller information utilizable to control selection of a particular configuration for the configurable switching element.

7. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 1 wherein the plurality of processor clients comprises N processor clients, and the plurality of memory instances comprises M memory instances, where N need not be equal to M.

8. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 7 wherein N is less than M.

9. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 1 wherein the configurable switching element is configurable to connect any one of the plurality of processor clients to any set of memory instances comprising one or more of the plurality of memory instances.

10. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 1 wherein for a given configuration of the configurable switching element, each of at least a subset of the memory instances has one and only one of the processor clients assigned to it.

11. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 1 wherein addresses are allocated to multiple memory instances associated with the given processor client in order of decreasing memory instance size.

12. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 1 wherein multiple memory instances associated with the given processor client have different sizes which are related to one another as multiples of two.

13. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 1 wherein a different set of mask bits is associated with each of a plurality of different memory instance sizes, and a different address decoder value is associated with each of the plurality of memory instances.

14. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 13 wherein address decoding logic applies the mask bits for a given memory instance to an incoming address from the given processor client, and compares the result to the address decoder value for the given memory instance to determine if the incoming address is directed to an address in the given memory instance.

15. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 14 wherein a decoded address is considered valid for the given processor client only if a master client identifier stored for the given memory instance specifies the given processor client.

16. (Currently amended) The ~~apparatus~~ network processor integrated circuit of claim 1 wherein the network processor integrated circuit is configured to provide an

interface for communication of protocol data units between a network and a switch fabric.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Currently amended) A method for use in a network processor integrated circuit for controlling access of a plurality of processor clients internal to the network processor integrated circuit to a plurality of memory instances of an internal memory of the network processor integrated circuit, the method comprising the steps of:

providing within the network processor integrated circuit an internal memory controller comprising a configurable switching element;

the configurable switching element being connectable between the plurality of processor clients and the plurality of memory instances and being operative to control access of particular ones of the plurality of processor clients to particular ones of the plurality of memory instances;

wherein the configurable switching element is configurable to connect any one of at least a subset of the plurality of processor clients to each of at least a subset of the plurality of memory instances; and

selecting one of at least a first selectable configuration and a second selectable configuration of the configurable switching element, wherein in the first selectable configuration a given one of the processor clients is permitted to access a first set of memory instances comprising one or more of the plurality of memory instances, and in the second selectable configuration the given processor client is permitted to access a second set of memory instances comprising one or more of the plurality of memory instances, the second set being different than the first set.